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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,300	04/22/2004	Yuichi Matsui	XA-10070	7208

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/829,300	MATSUI, YUICHI
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004 and 07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 20-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 20-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 09/07/2004 is acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a silicon oxide film" in "a silicon oxide film exists between said first electrode and said dielectric" of **claim 11** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-4, 8, 10, 23, 28, and 33** are rejected under 35 U.S.C. 102(b) as being anticipated by Nishioka U.S. Patent 5,970,337 (cited by Applicant, and hereinafter referred to as the '337 reference).

The '337 reference discloses in the figures, particularly Figs. 1, 2, 22, and 23, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device comprising:

a first conducting film (2/3, Figs. 1-2; or 103/104, Figs. 22-23) formed on a semiconductor substrate (1 or 101);

a dielectric (4/5 or "generally indicated at 105") deposited on said first conducting film; and

a second conducting film ("upper electrode", column 3, lines 55-60; or 107) formed on said dielectric, wherein said dielectric comprises a polycrystalline oxide (crystal "BST", "BST" for (Ba,Sr)TiO_3, column 1, lines 24-30) having a plurality of crystal grains and an amorphous oxide (amorphous STO, Fig. 2; or tantalum pentoxide, or Ta_2O_5, and note that as a crystallization temperature for tantalum pentoxide is about 750° C - as is known in the art and as disclosed by Applicant and by Matsui et al. U.S. Patent Application Publication 20030151083, paragraph [0005], which is cited by Applicant - and because the tantalum pentoxide is formed at about 400 to 500° C – the '337 reference, column 10, lines 35-45 - the tantalum pentoxide should remain in an amorphous state) present at the boundaries formed between said crystal grains (paragraph bridging columns 3 and 4, particularly "due to the cavities generated on the intergranular crystal boundaries of BST film 5...repair the defects by forming laminated ferroelectric films to fill the cavities").

Referring to **claim 4** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device having a capacitor comprising:

a first electrode (2/3) of said capacitor comprising a first conducting film formed on a semiconductor substrate;

a dielectric deposited on said first electrode; and

a second electrode of said capacitor comprising a second conducting film formed on said dielectric,

wherein the dielectric comprises a polycrystalline oxide having a plurality of crystal grains and an amorphous oxide present at boundaries formed between said crystal grains.

Referring to **claim 2** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device having a capacitor comprising:

semiconductor device comprising:

a first conducting film (103/104) formed on a semiconductor substrate;

a dielectric (generally indicated at 105) deposited on said first conducting film;

a second conducting film (107) formed on said dielectric,

wherein said dielectric comprises a polycrystalline oxide with a first crystallization temperature (about 650° C, column 3, lines 50-55, column 8, lines 30-35), having a plurality of crystal grains, and an amorphous oxide with a crystallization temperature (about 750° C, as noted above) higher than the first crystallization temperature (650° C, as just noted) present at boundaries formed between said crystal grains.

Referring to **claim 3** and using the same reference characters, interpretations, and citations as detailed above for claims 1 and 2 where applicable, the reference discloses a semiconductor device having a capacitor comprising:

semiconductor device comprising:

a first conducting film formed on a semiconductor substrate;

a dielectric deposited on said first conducting film; and

a second conducting film formed on said dielectric,

wherein said dielectric comprises a polycrystalline oxide with a first dielectric constant and first crystallization temperature, having a plurality of crystal grains, and an amorphous oxide, having a lower dielectric constant than said first dielectric constant (as is known in the art)

and a higher crystallization temperature than said first crystallization temperature, present at boundaries formed between said crystal grains.

Referring to **claims 8, 23, 28, and 33**, the reference further discloses that the amorphous oxide (STO) or the amorphous Ta_2O_5 comprises an oxide of titanium (column 4, lines 10-15, STO = $SrTiO_3$) or tantalum.

Referring to **claim 10**, the reference further discloses that said first electrode comprises platinum (Pt).

5. **Claims 1 and 4** are rejected under 35 U.S.C. 102(b) as being anticipated by SUENAGA et al. Japanese Patent JP02002016234A.

SUENAGA discloses in the translated SOLUTION Section a semiconductor device as claimed.

In reference to **claim 1**, SUENAGA discloses a semiconductor device comprising:

a first conducting film (inherent for the capacitor to function) formed on a semiconductor substrate (not shown);

a dielectric (12) deposited on said first conducting film; and

a second conducting film (inherent) formed on said dielectric, wherein said dielectric comprises a polycrystalline oxide ("ferroelectric") having a plurality of crystal grains and an amorphous oxide present at the boundaries formed between said crystal grains ("spaces between crystal grains (grain boundaries) of a ferroelectric thin film 12 in the capacitor are filled with fine crystals or amorphous grains").

Referring to **claim 4** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device having a capacitor comprising:

a first electrode of said capacitor comprising a first conducting film formed on a semiconductor substrate;

a dielectric deposited on said first electrode; and

a second electrode of said capacitor comprising a second conducting film formed on said dielectric,

wherein the dielectric comprises a polycrystalline oxide having a plurality of crystal grains and an amorphous oxide present at boundaries formed between said crystal grains.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 7,9,11,22,24,27,29,32 and 34** are rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka U.S. Patent 5,970,337 (cited by Applicant, and hereinafter referred to as the '337 reference).

Referring to **claims 7, 22, 27, and 32**, the '337 reference discloses a semiconductor device as claimed and as detailed above for claims 1-4 including the amorphous oxide (Ta_2O_5) in said dielectric. Although the reference does not disclose that the amorphous oxide in said

dielectric is from 5% to 50%, it appears that the amorphous oxide in said dielectric is from 5% to 50% (Fig. 23).

Referring to **claim 11**, the '337 reference discloses a semiconductor device including a capacitor as claimed and as detailed above for claim 4 including said first electrode formed of a metal. However, the reference teaches that the teachings could be applied to other type of capacitors (column 12, lines 40-46); and in particular, as the reference does not exclude the possibility of using polysilicon as a first electrode, polysilicon as a first electrode could be used, and because of the high temperature process in forming said dielectric layer, it would appear that the high temperature would form a silicon oxide as claimed.

Referring to **claims 9, 24, 29, and 34**, the '337 reference discloses a semiconductor device including a capacitor as claimed and as detailed above for claims 1-4, said capacitor including said dielectric having a film thickness. However, the reference does not teach a film thickness as claimed. Nevertheless, the reference discloses that the teachings could be applied to other type of capacitors (column 12, lines 40-46), and particularly does not exclude a particular range of thickness, such as a range of 5 nm to 20 nm as claimed; therefore a modification so as to obtain such a range of thickness would have been obvious to one of ordinary skill in the art.

7. **Claims 1-11 and 20-34** are rejected under 35 U.S.C. §103(a) as being unpatentable over Sakai Japanese Patent JP409017949A in view of knowledge in the art as disclosed by Ómori et al. U.S. Patent Application Publication 20040111849 or Yang et al. U.S. Patent Application Publication 20030102501 and further in view of knowledge in the art as disclosed by Matsui et

al. U.S. Patent Application Publication 20030151083 (cited by Applicant, and hereinafter referred to as the '083 reference).

Referring to **claims 1-4**, Sakai discloses in the translated Abstract Section and the translated Constitution Section of the JP409017949A reference (hereinafter the '949 reference) a semiconductor device substantially as claimed. Specifically, the '949 reference discloses a semiconductor device including a capacitor having a high dielectric constant film 14 between a pair of electrodes 13, 17, wherein the high dielectric constant film 14 is of polycrystalline structure and composed of crystal grains, a crystal phase 15 and an amorphous phase 16 are present together in the high dielectric constant film. The reference further discloses that amorphous element 16 is present at boundaries formed between said crystal grains of polycrystal element 15 ("thus the high dielectric constant film is of such crystal grain structure that a crystal grain boundary is destroyed by the amorphous phase 16").

However, the '949 reference does not appear to disclose a specific material for the crystal-phase element 15 and the amorphous-phase element 16.

Furthermore, the reference also does not appear to disclose that said amorphous-phase element 16 has a dielectric constant which is lower than that of the crystal-phase element 15, and that said amorphous-phase element 16 has a crystallization temperature which is higher than that of the crystal-phase element 15 as recited in **claims 2 and 3** ("wherein said dielectric comprises a polycrystalline oxide with a first dielectric constant and first crystallization temperature, having a plurality of crystal grains, and an amorphous oxide, having a lower dielectric constant than said first dielectric constant and a higher crystallization temperature than said first crystallization temperature, present at boundaries formed between said crystal grains").

Nevertheless, at the time the invention was made, Omori, in also disclosing a semiconductor device including a capacitor having a high dielectric constant film, discloses that tantalum pentaoxide ("tantalum oxide") and niobium pentoxide ("niobium oxide") are the preferred materials for the high dielectric constant film for semiconductor devices including a capacitor having a high dielectric constant film (paragraph [0003]). Also, at the time the invention was made, Yang, in also disclosing a semiconductor device including a capacitor having a high dielectric constant film, discloses that tantalum pentaoxide or niobium pentoxide are desirable materials for the dielectric film (paragraph [0021]) (in reference also to the materials of **claims 5-6, 20-21, 25-26, and 30-31; 8, 23, 28, and 33**).

Furthermore, at the time the invention was made, it was known that tantalum pentoxide has a crystallization temperature of about 750° C and that niobium pentoxide has a crystallization temperature of about 500° C, as disclosed in detailed by the '083 reference, paragraphs [0005] and [0012].

Putting the various knowledge together, it would appear that the '949 reference's amorphous-phase element 16 should be a tantalum pentoxide because tantalum pentoxide is a preferred or desirable material, as is known and as disclosed by Omori or Yang and as detailed above, and also because tantalum pentoxide has a crystallization temperature of about 750° C, which is higher than that of niobium pentoxide, which is about 500° C, so that when the crystal-phase element 15 becomes crystallized at about 500° C, the amorphous-phase element 16, which should be tantalum pentoxide, remains amorphous because it has a higher crystallization temperature; and that the '949 reference's crystal-phase element 15 should be a niobium pentoxide because niobium pentoxide is a preferred or desirable material, as is known and as

disclosed by Omori or Yang and as detailed above, and also because niobium pentoxide has a crystallization temperature of about 500° C, which is lower than that of tantalum pentoxide, which is about 750° C, so that when the crystal-phase element 15 becomes crystallized at about 500° C, the amorphous-phase element 16, which should be tantalum pentoxide, remains amorphous.

With respect to the limitation that the amorphous oxide has a dielectric constant lower than that of the polycrystalline oxide ("wherein said dielectric comprises a polycrystalline oxide with a first dielectric constant and first crystallization temperature, having a plurality of crystal grains, and an amorphous oxide, having a lower dielectric constant than said first dielectric constant and a higher crystallization temperature than said first crystallization temperature, present at boundaries formed between said crystal grains") the amorphous oxide should have a dielectric constant lower than that of the polycrystalline oxide, as is known in the art.

Referring to **claims 10-11**, although the '949 reference does not appear to teach that a material for the first electrode is copper, platinum or polysilicon, such utilization of known and available materials for the first electrode would have been obvious to one of ordinary skill in the art because the reference also does not appear to preclude such usage of known and available materials for the first electrode; and when the chosen material is polysilicon for the first electrode, it would appear that the high temperature that would require to form said dielectric layer would form a silicon oxide as claimed.

Referring to **claims 7, 22, 27, and 32**, the combined teachings disclose a semiconductor device as claimed and as detailed above for claims 1-4 including the amorphous oxide (Ta_2O_5) in said dielectric. Although the references do not disclose that the amorphous oxide in said

dielectric is from 5% to 50%, it appears that amorphous phase 16, which modified to be the amorphous oxide, in said dielectric is from 5% to 50% (see Fig. 1, the '949 reference).

Referring to **claims 9, 24, 29, and 34**, the '337 reference discloses a semiconductor device including a capacitor as claimed and as detailed above for claims 1-4, said capacitor including said dielectric having a film thickness. However, the reference does not teach a film thickness as claimed. Nevertheless, it appears that teachings does not exclude a particular range of thickness, such as a range of 5 nm to 20 nm as claimed; therefore a modification so as to obtain such a range of thickness would have been obvious to one of ordinary skill in the art at the time the invention was made.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
October 27, 2005